

SYSTEMS

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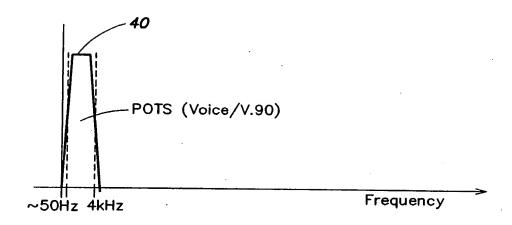
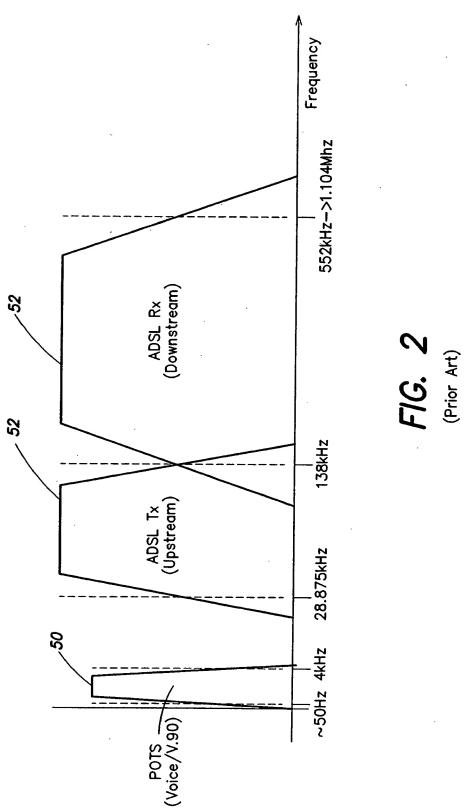
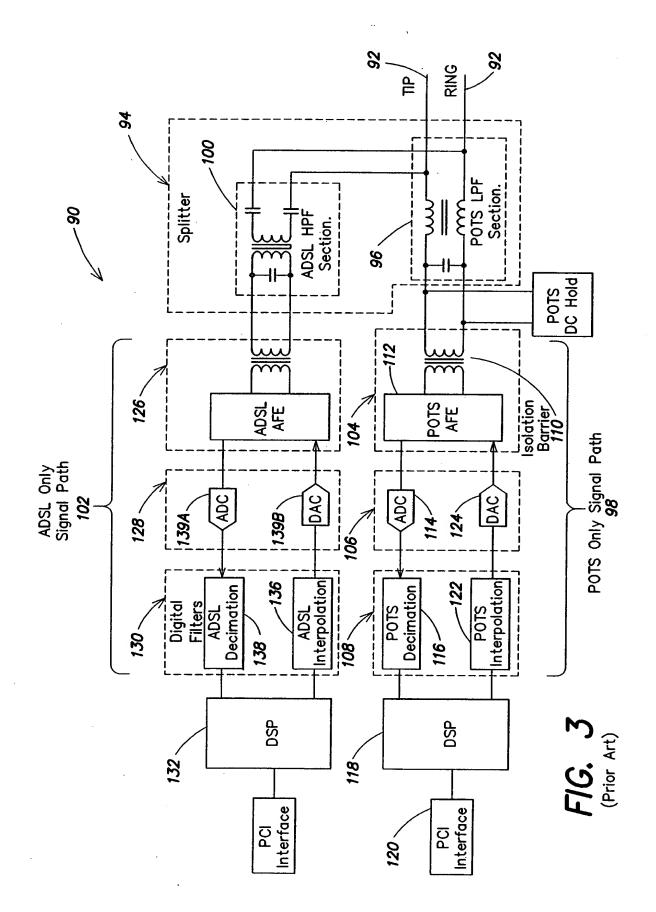


FIG. 1 (Prior Art)

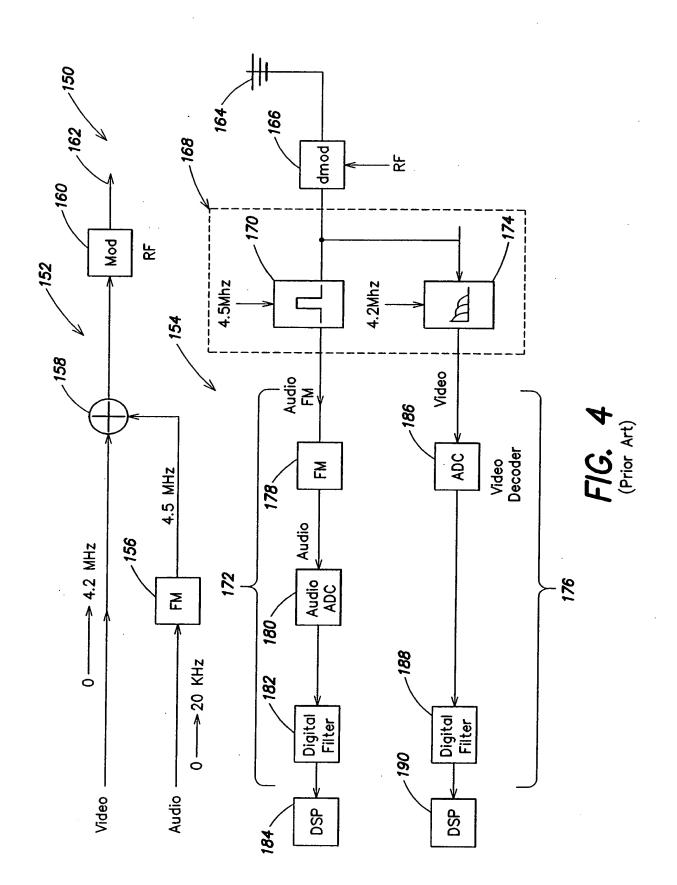


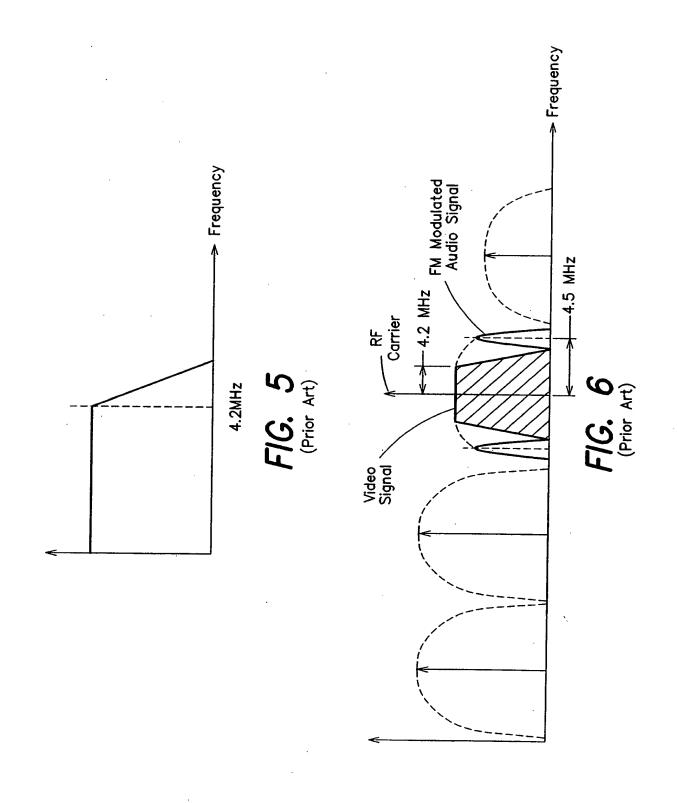
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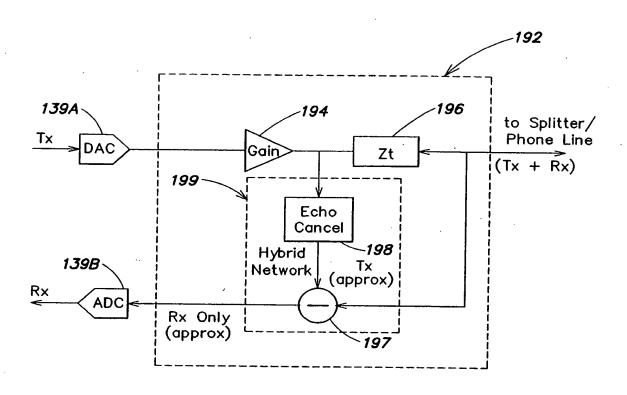


FIG. 7
(Prior Art)

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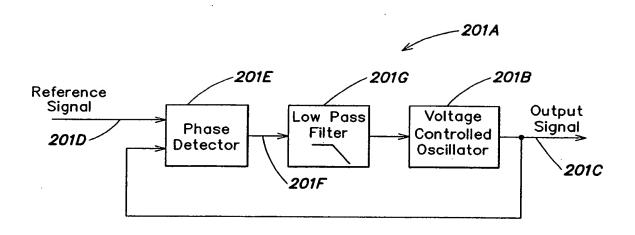
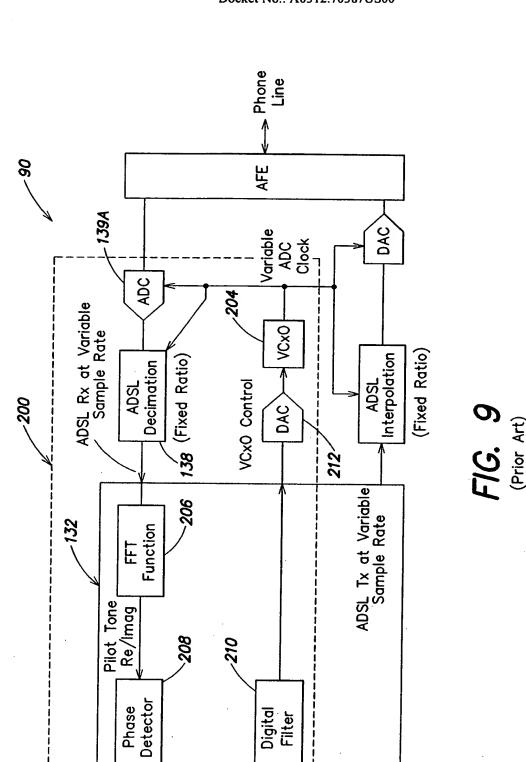


FIG. 8
(Prior Art)

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ADC Clock Up/Down

DSP

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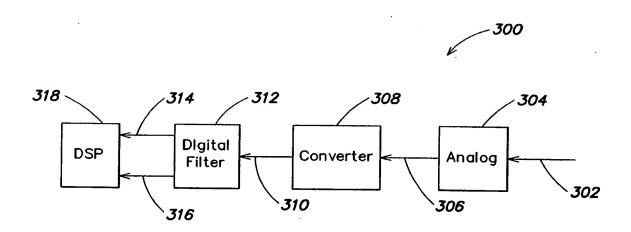
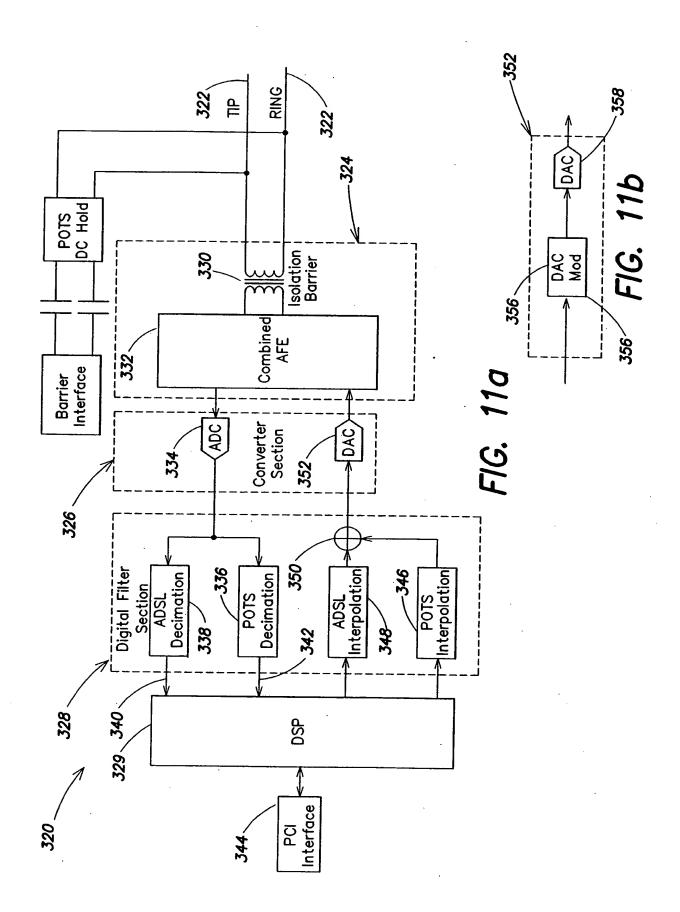
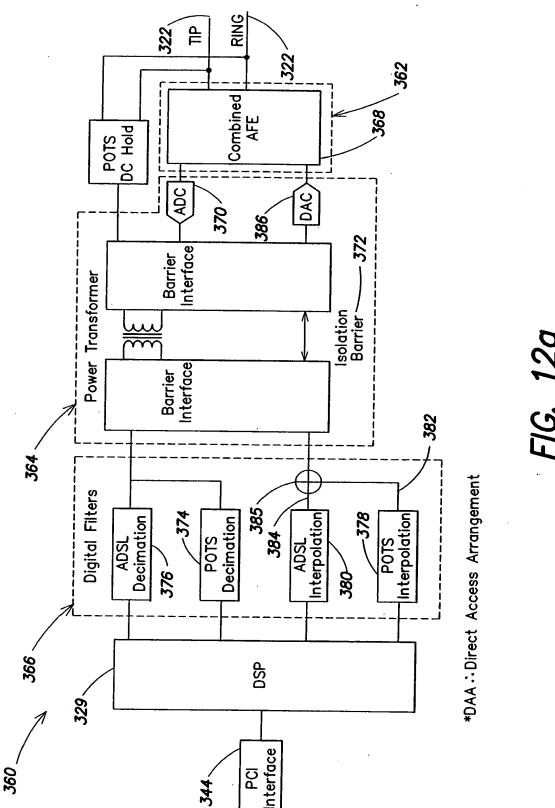


FIG. 10

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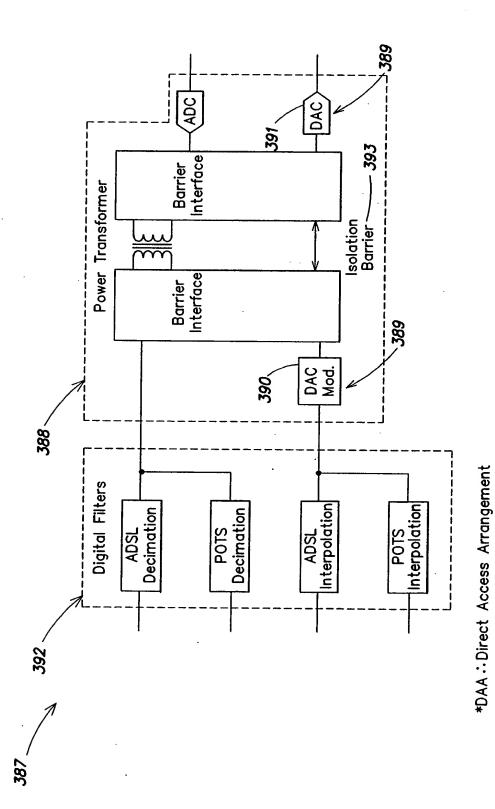


FIG. 12b

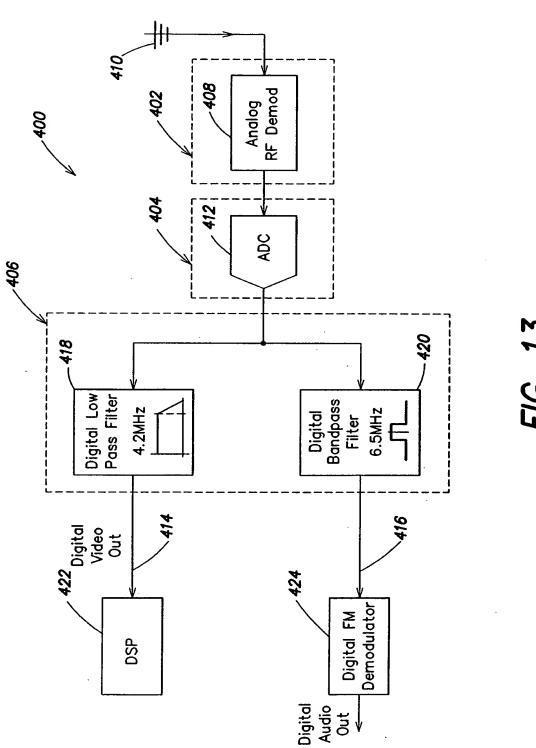
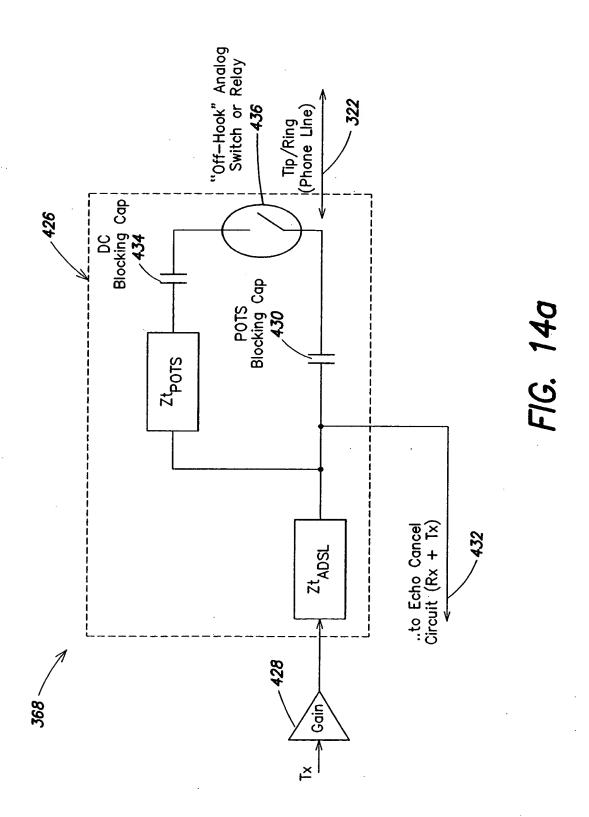
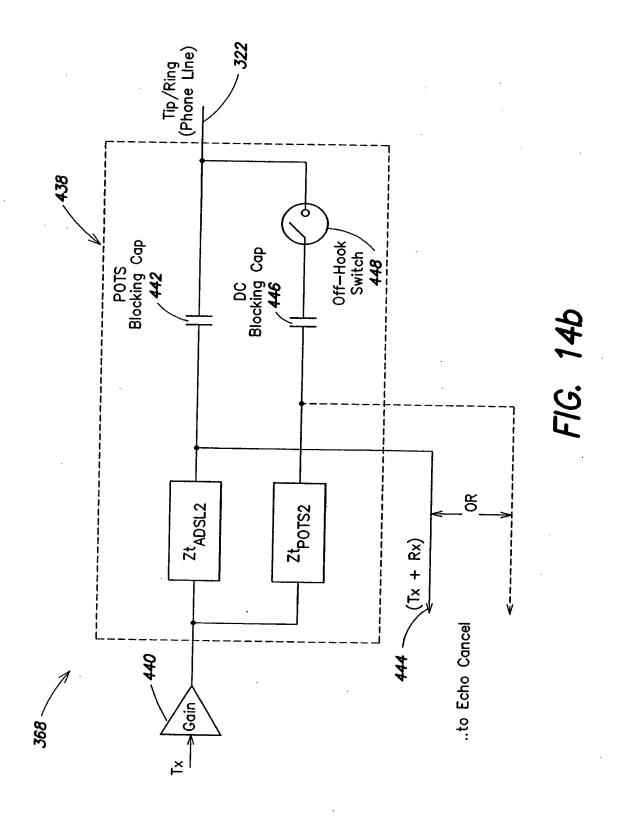


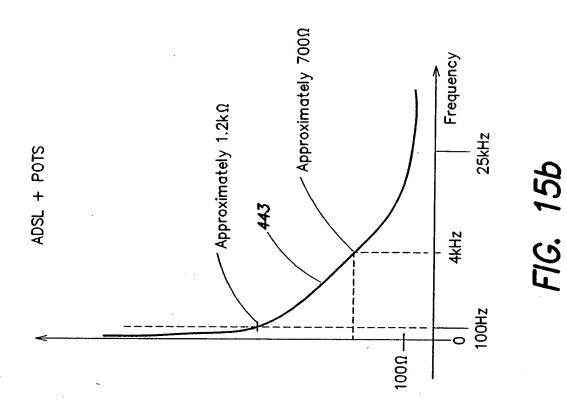
FIG. 13

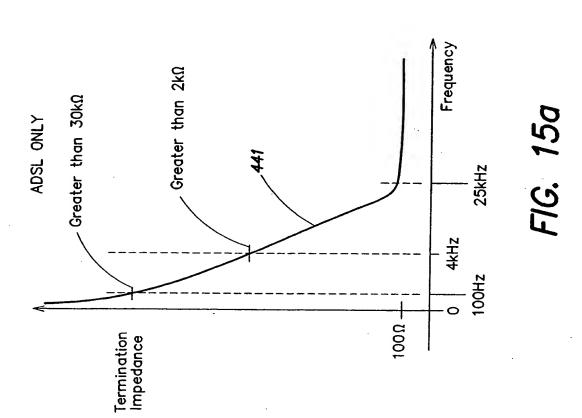
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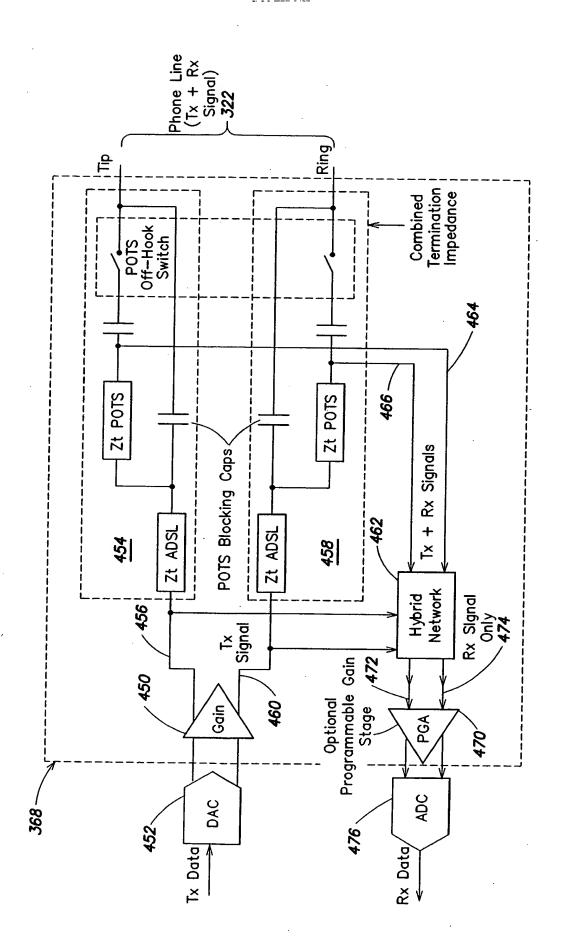
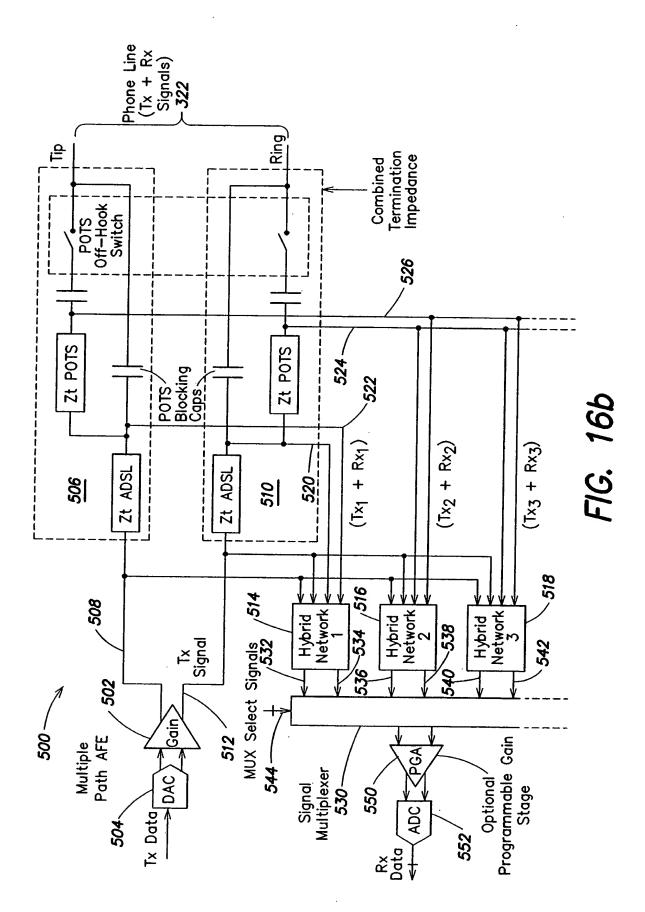


FIG. 16a



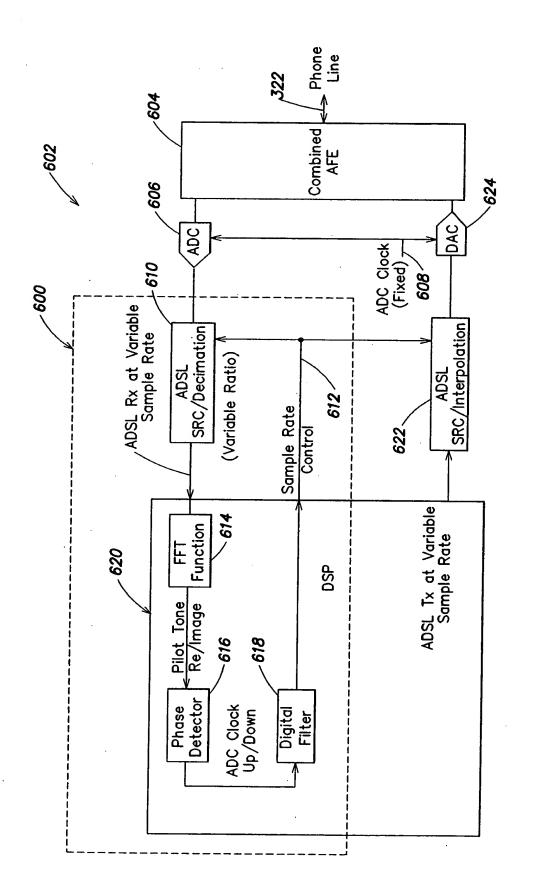


FIG. 17

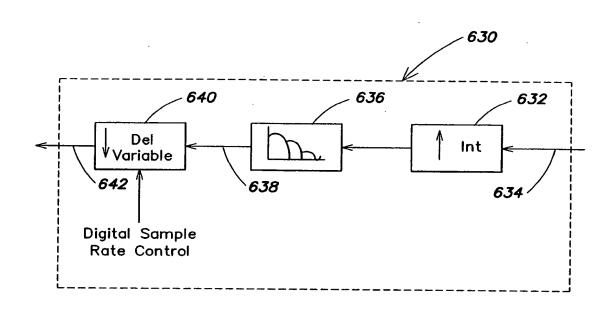


FIG. 18

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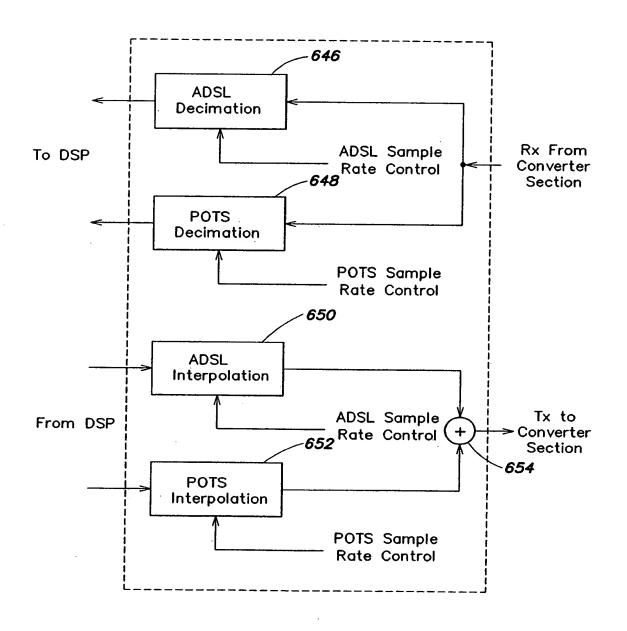
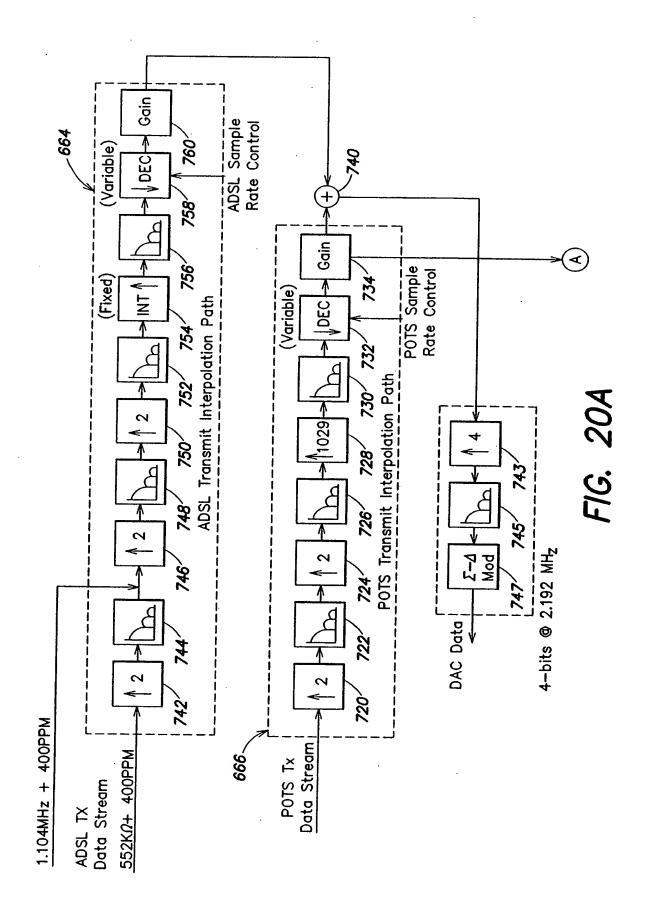
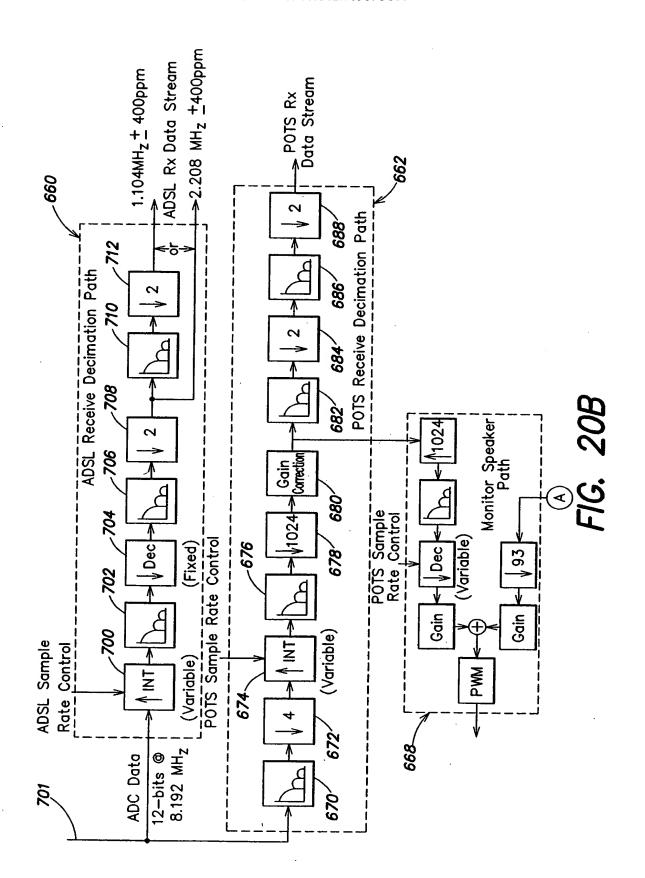


FIG. 19

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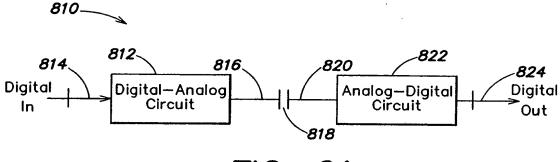


FIG. 21

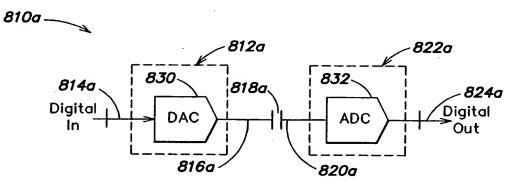


FIG. 22

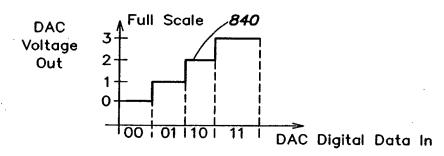


FIG. 23

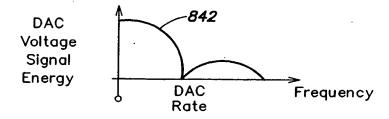
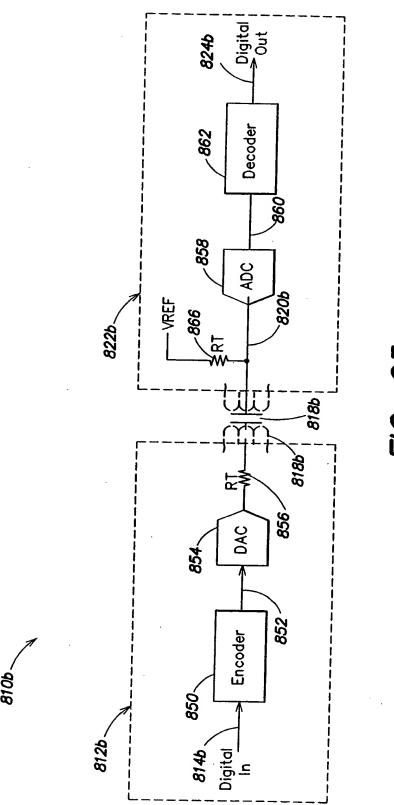


FIG. 24

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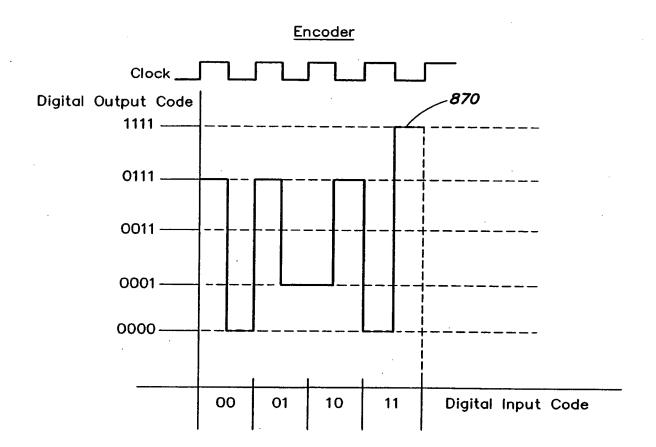


FIG. 26

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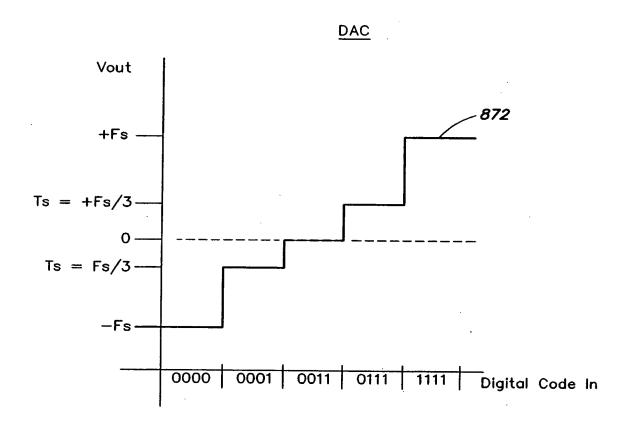


FIG. 27

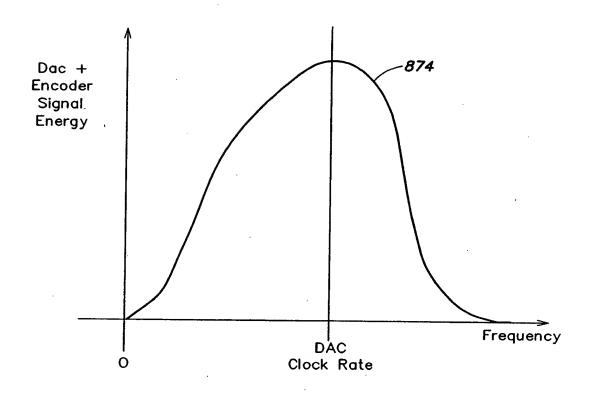
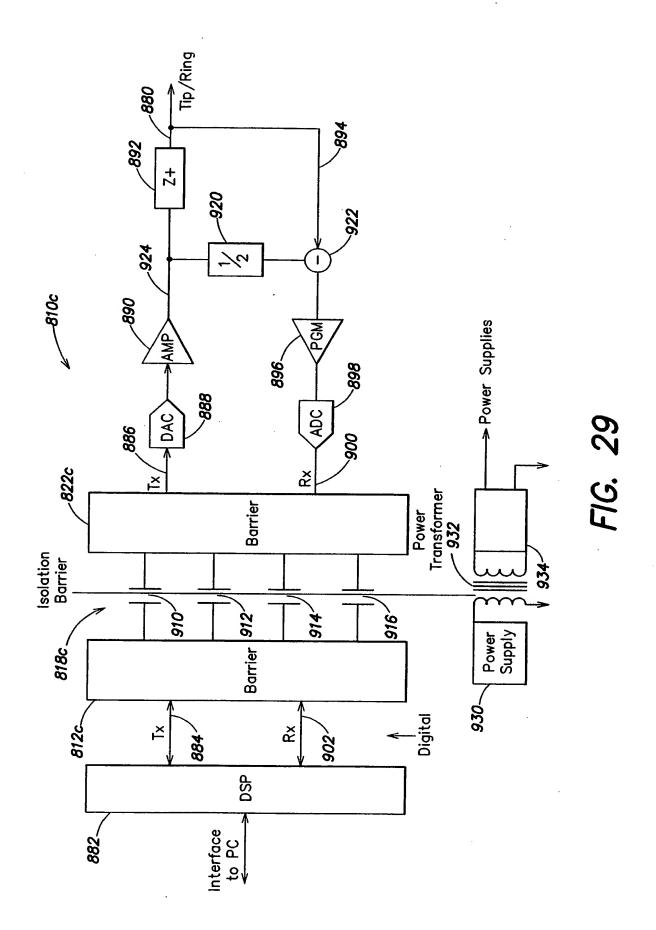
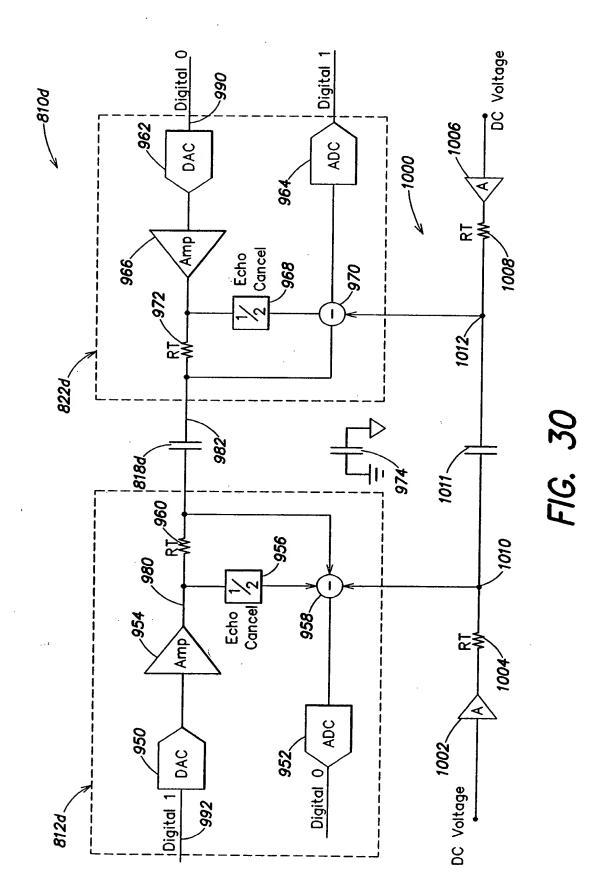


FIG. 28



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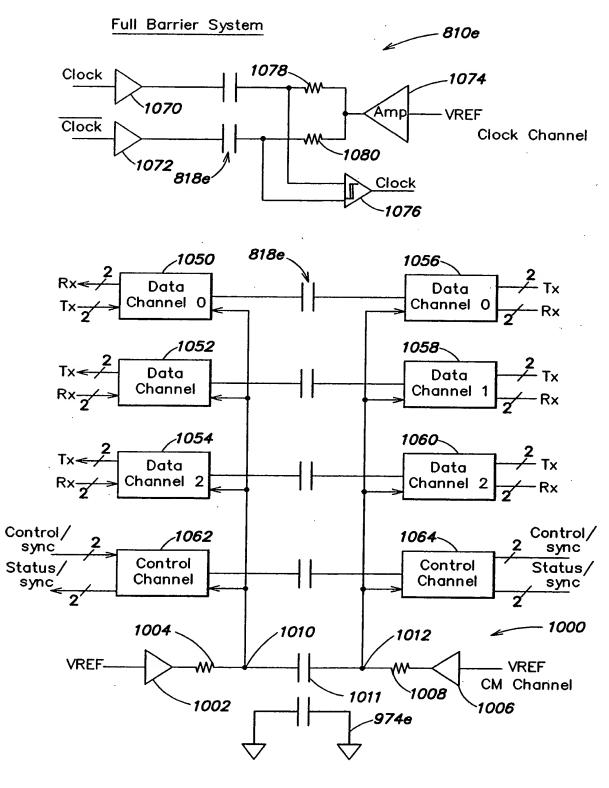


FIG. 31

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